Circuit Approaches to Nonlinear-ISI Mitigation in Noise-Shaped Bandpass D/A Conversion

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***Abstract*—This paper focuses on the analysis of nonlinear intersymbol interference (ISI) in RF bandpass delta-sigma power digital-to-analog converters (DACs). Digital RF transmitters based on direct delta-sigma modulation have been proposed for efficient linear multi-functional radios. We show that a realistic one-bit DAC limits the linearity of such a transmitter. The linearity is discussed in terms of ISI, for both single-ended and differential DAC circuits. Theoretical and experimental comparisons are given with a three-tone delta-sigma test signal at a 1.5 GHz clock frequency with 60 MHz possible signal bandwidth centered at 375 MHz. The signal-to-noise-and-distortion (SINAD) is shown to be improved for the differential case. It is also shown that circuit design and bias voltages have a dramatic effect on signal linearity.**

***Index Terms*—Nonlinear model, switching-mode, pulse modulation drain efficiency**

I. Introduction

INTEREST is increasing in "direct" digital RF transmitters that perform digital-to-analog (D/A) conversion at the transmitted UHF or microwave radio frequency (RF), with the goal of making analog frequency conversion unnecessary [1]–[3]. However, transmitting multiple, digitally summed signals simultaneously requires extraordinarily linear conversion to avoid intermodulation. In low-bandwidth baseband systems the linearity gold standard has long been $\Delta\Sigma$ D/A conversion [4], and the analogous RF system would be a digital RF transmitter using bandpass $\Delta\Sigma$ modulation as in Fig. 1(a) [5]–[9].

Conceptually, such a transmitter has three stages. A DSP-based bandpass $\Delta\Sigma$ modulator first converts the digital signal into one-bit form at a high sample rate. A one-bit power D/A converter (DAC) then converts that bit stream to the precise analog levels depicted in Fig. 1(b). The substantial quantization noise of this analog signal is spectrally shaped by the bandpass $\Delta\Sigma$ modulator into a signal-band noise floor notch between out-of-band noise shoulders as pictured in Fig. 1(c). Finally, bandpass filtering removes the noise shoulders.

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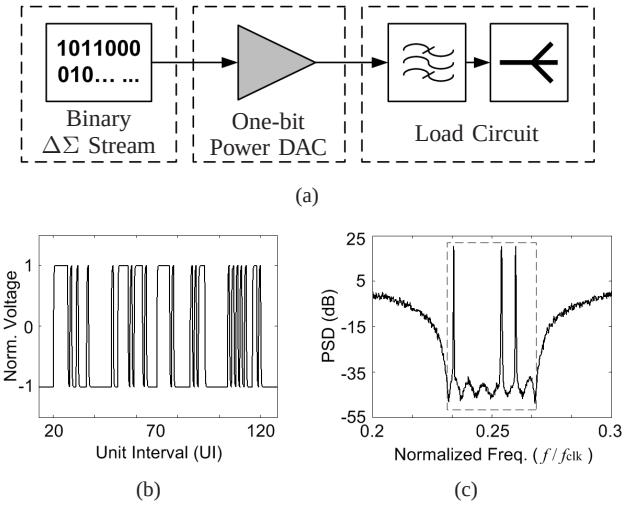


Fig. 1. Direct digital RF transmitter using bandpass $\Delta\Sigma$ modulation. (a) Block diagram. (b) Normalized one-bit-converter output. (c) Normalized output power spectral density (PSD) $f_{clk}S(f/f_{clk})$, where f_{clk} is the clock frequency of the digital bit sequence. Spectrum inside the dashed-line box represents the signal band.

This paper examines concepts and circuits for ultra-linear one-bit conversion at UHF clock rates using approaches scalable to microwave clock rates. We focus on nonlinear intersymbol interference (ISI) generated in an RF one-bit converter, which is shown to be a major consideration for $\Delta\Sigma$-based direct digital RF transmitter design.

A. Background in Nonlinear ISI

If the analog signal $s(t)$ is the output of the D/A conversion for the input binary digital bit sequence $d(n)$, for a linear time-invariant (LTI) D/A conversion, $s(t)$ can be written as

$$s(t) = \sum_n d(n)u(t - nT), \tag{1}$$

where T is the digital clock period, and $u(t)$ represents the analog unit pulse waveform. To simplify the notation in later derivations, $\overline{s}(t)$ is defined as the analog output of the D/A conversion when the input bit sequence is $-d(n)$.

Suppose the one-bit converter output looks like that in Fig. 2(a), with mirror image rise and fall waveforms that settle in less than the RF clock period T. In this case, the unit pulse $u(t)$ has width less than $2T$. The spectrum looks like the lower curve in Fig. 2(e). An output corresponding to nonideal conversion is shown in Fig. 2(b), with fall time shorter than

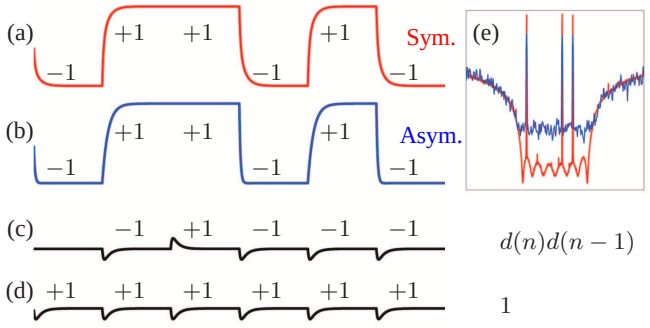


Fig. 2. Nonlinear ISI from the output waveform of a one-bit converter with one clock period of memory. (a) Symmetric rise/fall transition waveform. (b) Asymmetric rise, fall transition waveform. (c) Second-order nonlinear ISI component. (d) Data-independent component. (e) Normalized PSD for symmetric and asymmetric cases for a three-tone test signal (the axes limits and labels are the same as in Fig. 1(c)).

the rise time. This (b) waveform can be modeled as the sum of the (a), (c), and (d) waveforms:

$$\left.\begin{aligned} s(t) &= \sum_n d(n)u_1(t-nT) \end{aligned}\right\}\text{(a) linear term}$$

$$\left.\begin{aligned} &+ \sum_n d(n)d(n-1)u_2(t-nT) \end{aligned}\right\}\text{(c) } 2^{nd}\text{-order nonlinear term}$$

$$\left.\begin{aligned} &+ \sum_n u_0(t-nT) \end{aligned}\right\}\text{(d) data-indep. (nonlinear) term.} \quad (2)$$

Interference term (c) in (2) takes the form of LTI conversion of intersymbol product $d(n)d(n-1)$ and so is a type of nonlinear ISI. It raises the signal-band noise floor as shown in Fig. 2(e). In practice, very small asymmetries can raise the floor of a deep signal-band noise notch by 20 dB or more [10], [11].

Based on the Volterra series, which is often used in modeling nonlinear memory effects in power amplifiers [12], a special-case Wiener-Hammerstein system is used as a general model to describe the waveform-related nonlinear ISI effects in one-bit DAC circuits [10], [13]. Figure 3(a) illustrates the system: a cascade of an LTI discrete-time system, a memoryless nonlinear discrete-time system, and an LTI continuous-time system. An expanded model for one-bit DAC circuits is shown in Fig. 3(b). The binary input data fixes the first two subsystems in the model. Here, we focus on understanding nonlinear-ISI generation by examining how the third subsystem's waveforms relate to circuit topology.

To illustrate the fundamental generation of nonlinear ISI in a DAC, consider its simplest equivalent circuit in Fig. 4(a), where a DC bias current I_b is data-switched through the load. Simple memory in the form of a transmission-line delay can be added between the DAC and the load, as in Fig. 4(b). If the load is matched to the transmission line, the circuit in Fig. 4(b) reduces to (a), with no nonlinear ISI. Any mismatch spoils this perfect picture by reflecting the modulated forward current $i_+(t)$ from the load to create a modulated reverse current $i_-(t)$. The nonlinear ISI, as described above, is generated when the modulated reverse current is modulated again by the data-controlled switch. After N round trips an N^{th}-order nonlinear ISI component

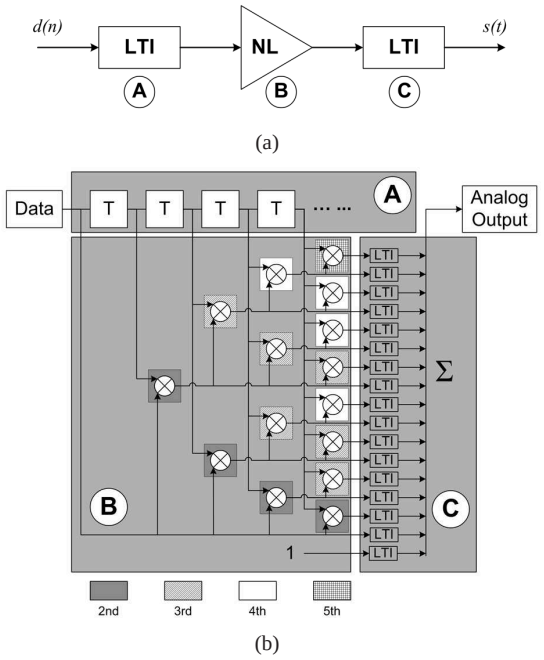


Fig. 3. (a) The general Wiener-Hammerstein model. (b) The special Wiener-Hammerstein nonlinear-ISI model for time-invariant D/A conversion. The model is parameterized by the memory length L and the unit pulse responses. The number of expansion terms of the model is equal to 2^L+1. The diagram shows an example with a memory of $L=4$ times clock period T. Each LTI output uses its own unit pulse response to map its discrete-time input data to the continuous-time output.

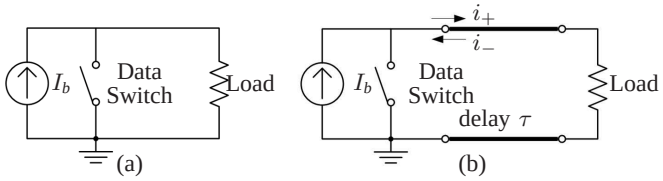


Fig. 4. Simple one-bit DAC ideal circuit models: (a) linear (b) nonlinear.

proportional to $\rho(t-\tau)\rho(t-3\tau)\cdots\rho(t-(2N-1)\tau)$ is presented at the load, where $\rho(t)$ represents the load reflection coefficient.

In this simple model, the transmission-line delay created the nonlinear ISI. As we will see later, load reactance can contribute delay that leads to nonlinear ISI in actual circuits.

B. Related Work and Outline

High frequency DACs have been a research topic for decades. An RF DAC with 60 dB in-band SNR measured at 942 MHz with 17.5 MHz bandwidth is demonstrated in [14]. This converter cannot be directly utilized for $\Delta\Sigma$ RF transmitters due to low output power and efficiency. Using switching-mode active devices with $\Delta\Sigma$ signals to achieve both high linearity and efficiency for power amplifiers (PA) is presented in [15], [16], where both simulated and measured results suggest that it is a promising approach. Different class-D PA topologies for one-bit bandpass $\Delta\Sigma$ D/A converters are compared in [17] in terms of power efficiency. Analytical design equations for an efficient RF complementary voltage-switched class-D amplifier with $\Delta\Sigma$ driven signals are derived in [18]. An H-bridge class-D PA with over 30% drain

efficiency when driven by a $\Delta\Sigma$ modulator is presented in [19], with a detailed analysis of the PA efficiency. GaAs-HBTs and GaN-HEMTs are used to implement switching-mode amplifiers and efficencies are compared under $\Delta\Sigma$ drive in [20]. Other high-efficiency 50% duty cycle switched-mode linearized RFPAs have been demostrated up to X-band in, e.g. [21], [22].

It can be seen that all the presented work on power amplification with nonlinear active devices and $\Delta\Sigma$ modulation at RF focuses on power efficiency of the active circuit. Signal linearity is largely ignored, even though the fundamental reason to explore $\Delta\Sigma$ conversion at RF is the hope of obtaining superior linearity, as is done at lower frequencies. Nonlinear ISI in a one-bit modulated DAC at RF has been studied only by Gupta and Collins in [23], [24]. In their novel approach, both measurement and mitigation of nonlinear ISI hinged on replacing $\Delta\Sigma$ modulation with an offline list-decoding process closely related to optimal Viterbi decoding of convolutional codes. However, the work did not examine circuit mechanisms that generate nonlinear ISI but treated the circuit as a black box with ISI characteristics to be measured and corrected.

The work presented in this paper examines and quantifies the generation of nonlinear ISI effects in the active circuits based on the nonlinear model in Fig. 3 and simplified DAC circuit models. Preliminary measurement results are presented to support the analysis. In order to draw attention to the signal linearity described by ISI, we refer to the active circuit as an RF power DAC instead of a PA.

The remainder of the paper is organized as follows:

- Section II and III present the theoretical analysis for one-bit single-ended (single-transistor) and differential power DACs based on general and simplified circuit models. Nonlinear ISI generation mechanisms are examined. Several DAC circuit topologies are compared.
- Section IV discusses the design of experimental single-ended and differential one-bit power-DAC circuits, along with the measurement parameters and setup.
- Section V presents the measurement results and comparisons to simulations.

II. Single-Ended One-Bit Power D/A Converter

In this section, based on an approximate circuit model for a single-ended power DAC, the signal at the output of the DAC is expressed in the time domain as the sum of subcurrents, related to different orders of nonlinear ISI terms. It is shown that, in the single-ended configuration, nonlinear ISI generated from the transistor switching conductance is hard to avoid if the switching process is not instantaneous, and nonlinear ISI generated from the load circuit is inevitable with the existence of reactive components.

The circuit diagram of a single-ended converter is shown in Fig. 5(a). Ideally, a transistor can be modeled as a perfect switch when it is driven by large binary digital signals. However, at RF frequencies, this model is inaccurate. A simplified circuit model for the converter is shown in Fig. 5(b). The transistor is modeled as a time varying conductance $g_S(t)$ in parallel with an output capacitance C. The input of the circuit

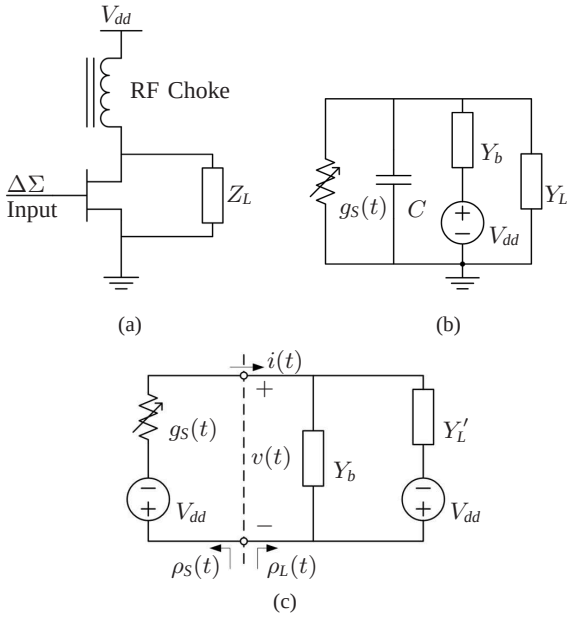


Fig. 5. Single-ended one-bit DAC (a) circuit diagram; (b) equivalent circuit model; (c) modified equivalent circuit model used in analysis. ($Y_L = 1/Z_L$)

is modeled by $g_S(t)$ which changes between the steady state conductances $g_{on}(t)$ and $g_{off}(t)$, with transitions $g_{rise}(t)$ and $g_{fall}(t)$. The output capacitance C is assumed to be linear and equal to C_{ds} in parallel with the series capacitance of C_{gs} and C_{gd}. Such an assumption is made based on the equivalent circuit for the MESFET/HEMT large-signal model [25], where the nonlinear capacitive components are only C_{gs} and C_{gd}, and $C_{gd} << C_{gs}, C_{ds}$. The bias RF choke is represented by Y_b. The DC block and the load are combined into Z_L (Y_L) in Fig. 5.

A. Current Solution at The Reference Plane

To better understand the converter-generated nonlinear ISI, an equivalent circuit model is formulated as in Fig. 5(c) by changing the reference ground, where

$$Y_L'(s) = Y_L(s) + sC. \tag{3}$$

In the equivalent circuit model, a reference plane — the dashed line — divides the circuit into a time-varying but memoryless source and an LTI load with reactive memory.

Key to the analysis below is the use of the alternative circuit variables $i^+(t)$ and $i^-(t)$ defined by the change-of-variable relationship

$$\begin{pmatrix} i(t) \\ v(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix} \begin{pmatrix} i^+(t) \\ i^-(t) \end{pmatrix}, \tag{4}$$

where R_{ref} is an arbitrary reference impedance. A proper choice of R_{ref} can simplify the nonlinear ISI analysis, which will be shown later. By writing KCL to characterize the source and load sides in the time and Laplace domains respectively, we obtain

$$i(t) = -g_S(t)\left(v(t) + V_{dd}\right), \tag{5}$$

$$I(s) = Y_t(s)V(s) + Y_L'(s)V_{dd}(s), \tag{6}$$

where

$$Y_t(s) = Y_b(s) + Y_L'(s). \tag{7}$$

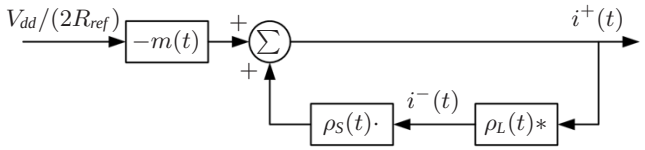


Fig. 6. Transfer function block diagram of $i^+(t)$. ('$\cdot$' denotes a time domain product, and '$*$' denotes a continuous-time convolution.)

If V_{dd} is an ideal DC voltage source, and the load circuit is AC coupled to the transistor, then in steady-state (6) can be simplified as

$$I(s) = Y_t(s)V(s). \tag{8}$$

After a change of variables, $i^+(t)$ and $i^-(t)$ are obtained:

$$i^+(t) = \rho_S(t)i^-(t) - m(t)V_{dd}/(2R_{ref}), \tag{9}$$
$$I^-(s) = \mathcal{R}_L(s)I^+(s), \tag{10}$$
$$i^-(t) = \rho_L(t) * i^+(t), \tag{11}$$

where

$$\rho_S(t) = (1 + R_{ref}g_S(t))^{-1}(1 - R_{ref}g_S(t)), \tag{12}$$
$$m(t) = (1 + R_{ref}g_S(t))^{-1}2R_{ref}g_S(t) = 1 - \rho_S(t), \tag{13}$$
$$\mathcal{R}_L(s) = (1 + R_{ref}Y_t(s))^{-1}(1 - R_{ref}Y_t(s)), \tag{14}$$

and $*$ denotes continuous-time convolution, while $\rho_L(t) \leftrightarrow \mathcal{R}_L(s)$ is a Laplace transform pair.

Based on (9) and (11), a transfer function block diagram is shown in Fig. 6, and an initial condition and recursion relationships can be defined as

$$i_0^+(t) = -m(t)V_{dd}/(2R_{ref}), \tag{15}$$
$$i_k^-(t) = \rho_L(t) * i_{k-1}^+(t), \tag{16}$$
$$i_k^+(t) = \rho_S(t)i_k^-(t), \tag{17}$$

where k represents the number of times that the initial signal circulates around the feedback loop. Now, $i^+(t)$ and $i^-(t)$ can be expressed in terms of the sum of subcurrents as

$$i^+(t) = \sum_{k=0}^{\infty} i_k^+(t), \tag{18}$$
$$i^-(t) = \sum_{k=1}^{\infty} i_k^-(t), \tag{19}$$

Therefore, the total current at the reference plane is

$$i(t) = \sum_{k=0}^{\infty} i_k^+(t) - \sum_{k=1}^{\infty} i_k^-(t). \tag{20}$$

Note that the expressions (12) and (14) are analogous to the reflection coefficients in transmission-line theory. However, the circuits from Fig. 5 that the analysis is based on consist purely of lumped elements.

B. Nonlinearities

Because the load circuit is LTI, the nonlinear ISI terms will first show up in $i^+(t)$. Using (18) and the nonlinear ISI model described in Section I, we next show how different parts of the converter create nonlinear ISI in the output signal and how the choice of R_{ref} affects the analysis.

1) Nonlinear ISI from the source: In order to analyze the nonlinear effects from the source side alone, we assume that there is no reflection from the load and

$$\begin{aligned} i^+(t) = i_0^+(t) &= -m(t)\frac{V_{dd}}{R_{ref}} \\ &= (\rho_S(t) - 1)\frac{V_{dd}}{R_{ref}}. \end{aligned} \tag{21}$$

If the transistor is fast enough, where the transition processes $g_{rise}(t)$ and $g_{fall}(t)$ are shorter than a clock period ($t < T$), then only a single clock period of memory will exist in $g_S(t)$. This translates to a switching device with relatively small parasitic capacitance. Then, based on the nonlinear ISI model shown in Fig. 3, $\rho_S(t)$ takes the form of (2). It can be seen that $\rho_S(t)$ can represent a linear D/A conversion only if $\rho_S(t) + \overline{\rho_S}(t) = 0$. Defining $\alpha(t) = 1/2\ln(R_{ref}g_S(t))$ allows $m(t)$ and $\rho_S(t)$ to be written as

$$m(t) = 1 + \tanh\alpha(t), \tag{22}$$
$$\rho_S(t) = -\tanh\alpha(t). \tag{23}$$

The linear D/A conversion condition for $\rho_S(t)$ is equivalent to $\alpha(t) + \overline{\alpha}(t) = 0$ and can be expanded as

$$R_{ref}^2 g_S(t)\overline{g_S}(t) = 1. \tag{24}$$

If $g_{rise}(t)$, $g_{fall}(t)$, $g_{on}(t)$, and $g_{off}(t)$ correspond to parts of the waveforms from Fig. 7(a), then (24) can be expressed as

$$R_{ref}^2 g_{rise}(t)g_{fall}(t) = 1, \tag{25}$$
$$R_{ref}^2 g_{on}(t)g_{off}(t) = 1. \tag{26}$$

Now, it can be easily seen that the symmetry of $\alpha(t)$ and $\overline{\alpha}(t)$ does not imply the symmetry of $g_S(t)$ and $\overline{g_S}(t)$, especially of the transition edges. This is illustrated by the example waveforms in Fig. 7(b) and (c).

In practice, the switching behavior of $R_{ref}g_S(t)$ is determined by the physical device parameters and the bias conditions. Using the single-ended configuration, it is difficult to provide the symmetric transition waveforms needed to make $\alpha(t)$ linear in $d(n)$. However, it is possible to reduce nonlinearity by tuning the bias conditions to improve symmetry or by choosing a faster device. The latter makes the nonlinear-ISI pulses in Fig. 2(c) shorter so that they contain less energy.

2) Nonlinear ISI from the load: In order to analyze the nonlinear effects from the load side alone, we assume that there is no nonlinear ISI from the source. Under this assumption, the total positive current can be shown to be of the form

$$\begin{aligned} i^+(t) = \frac{V_{dd}}{2R_{ref}}\Bigg(&\sum_n d(n)p_1(t - nT) \\ &+ \sum_{m>0}\sum_n d(n)d(n-m)p_2^m(t - nT) \\ &+ \sum_{\ell>m}\sum_{m>0}\sum_n d(n)d(n-m)d(n-\ell)p_3^{m,\ell}(t - nT) \\ &+ \cdots\Bigg). \end{aligned} \tag{27}$$

where $p(t)$ with different superscripts and subscripts represents different LTI unit pulse responses. Details of the derivation

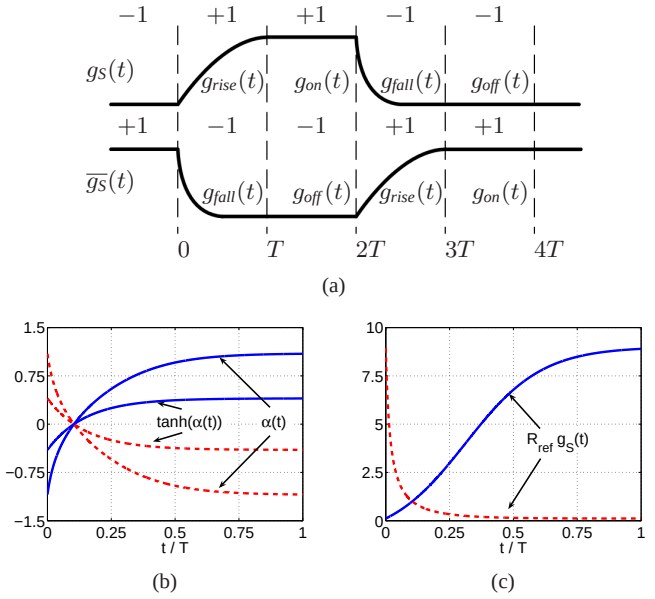


Fig. 7. (a) Illustration of $g_S(t)$ and $\overline{g_S}(t)$ asymmetries. (b) Rising and falling edge waveforms of $\tanh\alpha(t)$ and $\alpha(t)$, where $\alpha(t) = \ln(R_{ref}g_S(t))/2$. (c) Corresponding rising and falling edge waveforms of $R_{ref}g_S(t)$.

are given in Appendix A. The subscripts denote the response order, where the 0^{th} order is the data-independent response, the 1^{st} order is the linear response, and the 2^{nd} and higher orders are the nonlinear ISI responses. The superscripts indicate the time delay between the current bit and the interfered bits, measured in clock periods. The LTI unit pulse responses $p(t)$ are determined by $\rho_L(t)$ and $g_S(t)$.

It can be seen that the 0^{th} order term does not exist in (27), because the source side is assumed to be linear. In practice, the data-independent nonlinear term can occur at the output of the DAC as a result of clock feed-through.

It is shown in Appendix A that $\rho_L(t) \neq 0$, therefore $p(t)$ for 2^{nd} and high order terms in (27) is not zero and nonlinear ISI exists. The load models the actual load circuit combined with the output capacitance of the transistor and the bias circuit. Even for the ideal case of a purely resistive load and an ideal bias circuit, the capacitance causes memory and stretches the pulse shape, which generates intersymbol interference. Therefore, nonlinear effects are unavoidable in a single-switch converter.

C. Choosing R_{ref}

As mentioned previously, R_{ref} is an arbitrary intermediate parameter in (4). However, its value does affect how complicated the series expansion formulation is. For example, when $Y_t(s) = R_L^{-1}$ reflections from the load circuit can be completely suppressed by choosing $R_{ref} = R_L$ so that $\rho_L = 0$. The total current at the reference plane reduces to (21).

If R_{ref} is chosen to be different from R_L, definitions of (12) and (14) imply that both $\rho_S(t)$ and $\rho_L(t)$ are nonzero. In order to solve for $i(t)$, full series expansions of $i^+(t)$ and $i^-(t)$ are needed. However, these two cases represent the same physical circuit and so have the same current $i(t)$. Thus, in the second case, cancellation takes place between various terms of (21). A good choice of R_{ref} favors lower-order terms rather than higher-order terms that cancel.

III. Differential One-Bit Power D/A Converter

Nonlinear analysis of RF circuits usually deals with memoryless power nonlinearities, and the even-order nonlinear terms cancelled by differential circuits involve products of signals at a common time instant. Here it is nonlinear memory that is of interest, and the nonlinear terms involve products of data bits from different clock periods. Can differential configurations cancel nonlinear terms in this case as well?

In this section, following the same analysis procedure as in the previous section, nonlinear ISI effects inside a differential one-bit converter are examined and presented. It is shown that, compared to the single-ended case, differential one-bit power DACs can eliminate nonlinear ISI effects generated from the transistor switching conductance if relatively fast and identical transistors are used, and they can remove even-order nonlinear ISI terms generated from the load circuit if that load is properly balanced.

First, we define even- and odd-mode variables as

$$var_\Sigma = var_1 + var_2, \tag{28}$$

$$var_\Delta = var_1 - var_2. \tag{29}$$

The circuit diagram of a differential one-bit power DAC is shown in Fig. 8(a). By modeling the transistors and the bias circuits in the same way as in the single-ended case, the simplified circuit model shown in Fig. 8(b) is obtained. The components inside the dashed-line box can be treated as a two-port network, and its Y-parameters follow the relationship

$$[Y_L'(s)] = \begin{bmatrix} sC_1 + Y_L(s) & -Y_L(s) \\ -Y_L(s) & sC_2 + Y_L(s) \end{bmatrix}. \tag{30}$$

Again, by changing the reference ground, an equivalent circuit model, shown in Fig. 8(c), is formulated.

A. Current Solution at The Reference Plane

As in the singled-ended case, the transfer function block diagram in Fig. 6 can be used for the differential converter. Instead of scalars, V_{dd}, $i^+(t)$, and $i^-(t)$ become 2×1 vectors; $m(t)$, $\rho_S(t)$ and $\rho_L(t)$ become 2×2 matrices. The current components of the even- and odd-modes at the reference plane are derived in Appendix B. Again, $[i^+(t)]$ and $[i^-(t)]$ can be expressed as

$$\begin{pmatrix} i^+_\Sigma(t) \\ i^+_\Delta(t) \end{pmatrix} = \sum_{k=0}^{\infty} \begin{pmatrix} i^+_{\Sigma k}(t) \\ i^+_{\Delta k}(t) \end{pmatrix}, \tag{31}$$

$$\begin{pmatrix} i^-_\Sigma(t) \\ i^-_\Delta(t) \end{pmatrix} = \sum_{k=1}^{\infty} \begin{pmatrix} i^-_{\Sigma k}(t) \\ i^-_{\Delta k}(t) \end{pmatrix}, \tag{32}$$

with the recursion relationship

$$\begin{pmatrix} i^+_{\Sigma 0}(t) \\ i^+_{\Delta 0}(t) \end{pmatrix} = -[m(t)]\frac{1}{2R_{ref}} \begin{pmatrix} V_{dd\Sigma} \\ V_{dd\Delta} \end{pmatrix}, \tag{33}$$

$$\begin{pmatrix} i^-_{\Sigma k}(t) \\ i^-_{\Delta k}(t) \end{pmatrix} = [\rho_L(t)] * \begin{pmatrix} i^+_{\Sigma(k-1)}(t) \\ i^+_{\Delta(k-1)}(t) \end{pmatrix}, \tag{34}$$

$$\begin{pmatrix} i^+_{\Sigma k}(t) \\ i^+_{\Delta k}(t) \end{pmatrix} = [\rho_S(t)] \begin{pmatrix} i^-_{\Sigma k}(t) \\ i^-_{\Delta k}(t) \end{pmatrix}, \tag{35}$$

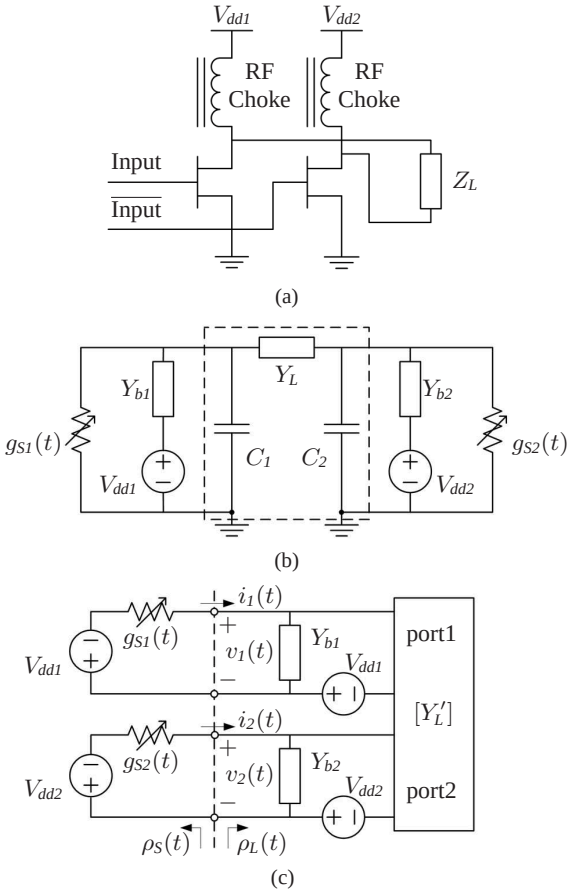


Fig. 8. Differential one-bit converter (a) circuit diagram; (b) equivalent circuit model; (c) modified equivalent circuit model used in analysis. The components in the dashed box in (b) are shown as the 2-port network in (c).

where the expressions for $[m(t)]$, $[\rho_L(t)]$, and $[\rho_S(t)]$ are shown in Appendix B. The total current at the reference plane is

$$\begin{pmatrix} i_\Sigma(t) \\ i_\Delta(t) \end{pmatrix} = \sum_{k=0}^{\infty} \begin{pmatrix} i^+_{\Sigma k}(t) \\ i^+_{\Delta k}(t) \end{pmatrix} - \sum_{k=1}^{\infty} \begin{pmatrix} i^-_{\Sigma k}(t) \\ i^-_{\Delta k}(t) \end{pmatrix}. \quad (36)$$

B. Nonlinearities

Again, we show how different parts of the differential converter affect the output signal quality based on the positive-current solution and the nonlinear ISI model. We focus on the odd-mode positive current, since it is the desired signal in this type of circuit. The analysis of the nonlinear ISI from the source and the load is done under the condition that the components in the two branches of the differential driver are identical, which means $V_{dd1} = V_{dd2} = V_{dd}$, $g_{S1}(t) = \overline{g_{S2}}(t)$, $Y_{b1}(s) = Y_{b2}(s) = Y_b(s)$, and $C_1 = C_2 = C$. Nonlinear effects caused by component mismatch are addressed later.

1) Nonlinear ISI from the source: If $[\rho_L] = 0$, the total $[i^+(t)]$ is

$$\begin{pmatrix} i^+_\Sigma(t) \\ i^+_\Delta(t) \end{pmatrix} = \begin{pmatrix} i^+_{\Sigma 0}(t) \\ i^+_{\Delta 0}(t) \end{pmatrix} = -[m(t)] \frac{1}{2R_{ref}} \begin{pmatrix} V_{dd\Sigma} \\ V_{dd\Delta} \end{pmatrix}. \quad (37)$$

The general expression for $[m(t)]$ is

$$[m(t)] = \begin{bmatrix} m^{cc}(t) & m^{dc}(t) \\ m^{dc}(t) & m^{cc}(t) \end{bmatrix} \quad (38)$$

where, after some algebra,

$$m^{cc}(t) = \frac{1}{2}\left(\frac{2R_{ref}\,g_{S1}(t)}{1+R_{ref}\,g_{S1}(t)} + \frac{2R_{ref}\,g_{S2}(t)}{1+R_{ref}\,g_{S2}(t)}\right), \quad (39)$$

$$m^{dc}(t) = -\frac{1}{2}\left(\frac{2}{1+R_{ref}\,g_{S1}(t)} - \frac{2}{1+R_{ref}\,g_{S2}(t)}\right). \quad (40)$$

When the transistors and bias circuits in the differential converter are identical, each element of $[i^+(t)]$ in (37) can be expanded as

$$i^+_\Sigma(t) = -\left(\frac{R_{ref}\,g_{S1}(t)}{1+R_{ref}\,g_{S1}(t)} + \frac{R_{ref}\,\overline{g_{S1}}(t)}{1+R_{ref}\,\overline{g_{S1}}(t)}\right)\frac{V_{dd}}{R_{ref}}, \quad (41)$$

$$i^+_\Delta(t) = \left(\frac{1}{1+R_{ref}\,g_{S1}(t)} - \frac{1}{1+R_{ref}\,\overline{g_{S1}}(t)}\right)\frac{V_{dd}}{R_{ref}}. \quad (42)$$

It can be seen that, as expected for a purely differential circuit,

$$\overline{i^+_\Sigma}(t) = \quad i^+_\Sigma(t), \quad (43)$$

$$\overline{i^+_\Delta}(t) = -i^+_\Delta(t). \quad (44)$$

If the transistors switch fast enough and the transitions of $g_S(t)$ are confined to one clock period, as was assumed for the single-ended converter, both even- and odd-mode currents take the form of (2). Then, based on (43) and (44), $i^+_\Sigma(t)$ and $i^+_\Delta(t)$ are simplified as

$$i^+_\Sigma(t) = \frac{V_{dd}}{R_{ref}}\left(\sum_n u_0(t-nT) + \sum_n d(n)d(n-1)u_2(t-nT)\right), \quad (45)$$

$$i^+_\Delta(t) = \frac{V_{dd}}{R_{ref}}\sum_n d(n)u_1(t-nT). \quad (46)$$

Thus, we can finally conclude that when the circuit components in the differential driver are identical and the transistors are relatively fast, the positive odd-mode current exhibits no nonlinear ISI. This is achieved with no symmetry requirement on $g_S(t)$.

2) Nonlinear ISI from the load: Assuming perfect matching of transistors and bias circuits, the transfer-function diagram in Fig. 6 can be expanded using (33), (34), and (35) into the form shown in Fig. 9. The superscripted components of $\rho_S(t)$ and $\rho_L(t)$ shown in the figure follow the notation from Appendix C, which also shows that expressions for $i^+_\Sigma(t)$ and $i^+_\Delta(t)$ have the forms

$$i^+_\Sigma(t) = \frac{V_{dd}}{R_{ref}}\Bigg(\sum_n p_0(t-nT) + \sum_{m>0}\sum_n d(n)d(n-m)p_2^m(t-nT) + \sum_{j>\ell}\sum_{\ell>m}\sum_{m>0}\sum_n d(n)d(n-m)d(n-\ell)d(n-j) \cdot p_4^{m,\ell,j}(t-nT) + \cdots\Bigg), \quad (47)$$

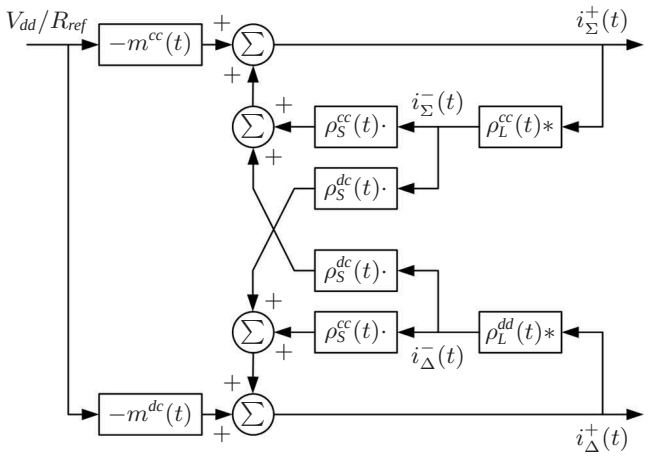


Fig. 9. Expanded transfer function block diagram of the differential one-bit converter when the transistors and bias circuits are identical.

$$i^+_\Delta(t) = \frac{V_{dd}}{R_{ref}}\Bigg(\sum_n d(n)p_1(t-nT) + \sum_{\ell>m}\sum_{m>0}\sum_n d(n)d(n-m)d(n-\ell)p_3^{m,\ell}(t-nT) + \cdots\Bigg). \quad (48)$$

The even- and odd-mode nonlinear terms in the above equations are completely separated. Since the load is differential, $i^+_\Sigma(t)$ is rejected, and only odd-order nonlinear terms in $i^+_\Delta(t)$ are transmitted. Therefore, nonlinear effects from the load reflection are reduced in the differential converter compared to the single-ended case.

3) Nonlinear ISI from component mismatch: When the components inside the differential pair are identical, the differential driver has substantial advantages over the single-ended driver in terms of output signal linearity. However, if it fails to satisfy such a condition, nonlinearities will be generated. For instance, when the two transistors are mismatched, the 2^{nd} order nonlinearity will be generated in the odd-mode current from the source circuit because $g_{S1}(t) \neq \overline{g_{S2}}(t)$, and even-order nonlinearities will be generated from the load circuit because $C_1 \neq C_2$.

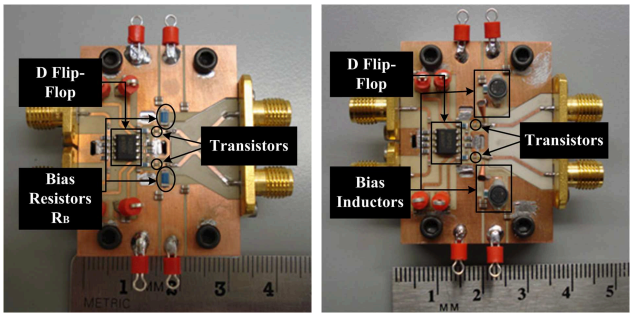
Nonlinear effects due to component mismatch can be quantified with a derivation considerably more cumbersome than the ones above though similar in spirit. The conclusion, however, is that in differential driver design it is important to consider the effects of component mismatch on linearity, but it will be easier to quantify these with specific transistor models through circuit simulations.

IV. One-bit Power D/A Converters Design and Measure

To experimentally evaluate and compare single-ended and differential one-bit power DACs, several circuits are fabricated and characterized. Design concerns, measurement parameters and procedures are briefly explained in the rest of the section.

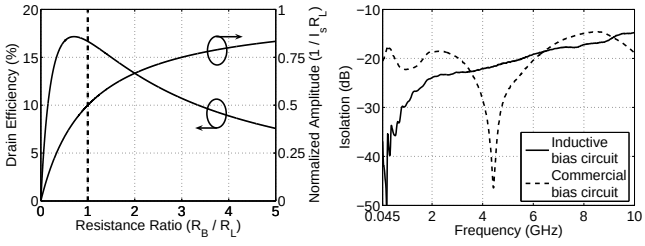
A. Converter Design

Hybrid circuits, as shown in Fig. 10, are designed on Rogers TMM substrate, with $\epsilon_r = 3.27$ and 0.381-mm thick, and



(a) (b)

Fig. 10. Photographs resistively biased (a) and inductively biased (b) differential converter circuits.



(a) (b)

Fig. 11. (a) Single-ended resistively biased converter efficiency and voltage swing as a function of the ratio of bias and load resistors (R_B/R_L). The dashed line shows $R_B = R_L = 50\,\Omega$ chosen for the design in this work. (b) Measured isolation of inductively biased circuit, compared to a broadband commercial bias circuit [26], exhibits the desired flat frequency response.

TriQuint (TGF2022-06) power pHEMTs. The goal of the input-circuit design is to maximize the transistor switching speed and thus reduce nonlinear ISI generated from the time-varying conductance $g_S(t)$. A broadband bias circuit is critical and can be either resistive or inductive. The lossy resistive bias circuit, Fig. 10(a), provides a constant response over a broad bandwidth, while the inductive bias circuit, Fig. 10(b), has inherent bandwidth limitations. To understand the trade-off between signal quality and efficiency, both types of bias circuits are designed and characterized.

For a resistively biased DAC, by modeling the transistor as an ideal switch and the load as a pure resistor R_L, the output signal peak-to-peak voltage V_{pp} and the pulse-modulation drain efficiency η_{PMD} can be expressed in terms of the bias resistor R_B. The following relationships are obtained,

$$V_{pp} = I_s R_L \frac{R_B}{R_B + R_L}, \quad (49)$$

$$\eta_{PMD} = \frac{R_B R_L}{(R_B + R_L)^2 + R_B^2 + R_B R_L}, \quad (50)$$

where I_s is the saturation current of the transistor. The output peak-to-peak voltage, normalized to $I_s R_L$, and the pulse-modulation drain efficiency are plotted versus R_B/R_L, in Fig. 11(a). The resistor value is chosen as $R_B = R_L = 50\,\Omega$ for higher efficiency with some sacrifice in the voltage range.

A broadband inductive bias circuit is designed with an $8\,\mu$H broadband conical inductor resonant around 40 GHz, in series with a 1 mH inductor and a parallel $1\,\text{k}\Omega$ resistor that damps the parasitic resonances. The isolation performance of the inductive bias tee is compared to a commercial component [26] in Fig. 11(b), showing a flat frequency response of the

RF-DC isolation.

The digital input signal to the designed DAC is provided by an FPGA as discussed in the next section. A differential data and clock D flip-flop chip from On Semiconductor (MC100EP52) with standard emitter-coupled logic is used as a buffer stage, with 800 mV peak-to-peak output across a 50 Ω termination.

B. Measurement Parameters

Since the one-bit converter characterization is different from that of conventional amplifiers, a few measurement parameters are specifically chosen and explained below.

1) Signal-to-noise-and-distortion (SINAD or SNDR) is the ratio of the signal to the noise-and-distortion component inside the signal band. This common DAC metric provides a measure of linearity, and it is calculated from a spectrum analyzer measurement. Several reasons make spectral measures of nonlinear ISI better than simple measurements of eye diagrams or other time-domain waveforms. First, the frequency spectrum of a $\Delta\Sigma$ modulated signal is more sensitive to nonlinear ISI. As shown in [10], [11], a slight change in the signal waveform can cause the noise floor in the signal band to shift dramatically. Second, parasitics of the probe are not negligible at RF frequencies, which makes real-time waveforms capturing a real challenge. Last, although a sampling scope can record very fast waveforms provided the right trigger signal, the time length of the recorded waveform is not long enough for an accurate spectrum estimation.

Standard linearity measures in PA characterization are not used here. Some of those, such as IP3 and IP5, assume power-law nonlinearities and thus are not relevant to a one-bit RF DAC. Others, such as ACPR and EVM, can be used to characterize linearity for specific applications but are less useful in understanding and predicting the fundamental underlying nonlinear effects.

2) Output signal RMS voltage (V_{RMS}) is the DAC output voltage into a $50\,\Omega$ load measured by an oscilloscope.

3) Pulse-modulation drain efficiency (η_{PMD}) is the ratio of the output pulse waveform power to the drain bias DC power. The pulse waveform power is calculated based on V_{RMS} and the load resistance. This parameter is different from the conventional amplifier drain efficiency, because the $\Delta\Sigma$ pulse waveform contains both signal and noise power. In order to measure the conventional drain efficiency of the DAC, signal filtering would be needed. Pulse-modulation drain efficiency is used here to calculate the losses inside the bias circuit and the transistor.

C. Measurement Setup

The measurement setup block diagram is shown in Fig. 12. A Xilinx Virtex-II Pro XC2VP30 FPGA development board is used for streaming the precomputed $\Delta\Sigma$ bit sequences to the converter. The data sequences are generated offline using an error-feedback $\Delta\Sigma$ loop with quantizer dithering [4] and a custom FIR loop filter [27]. The board has RocketIO™ differential serial transceivers capable of a 3.125 Gb/s transmit rate, as well as DDR memory to support large throughput

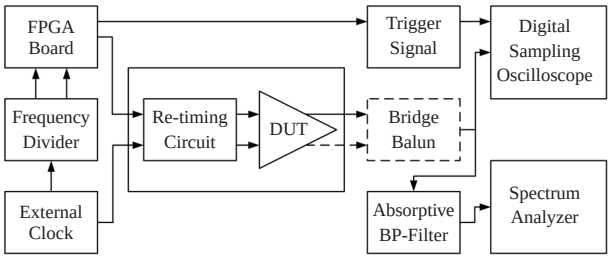


Fig. 12. Measurement setup block diagram. The $\Delta\Sigma$ modulated one-bit digital signal is fed into the power DAC from an externally clocked FPGA board. A D flip-flop is inserted at the input of the DAC to reduce random jitter. Measurement results in time and frequency domains are recorded by an oscilloscope and a spectrum analyzer, respectively. A bridge balun circuit is used for the differential measurement setup.

requirements. Because of the speed limit of the front bus connecting DDR and DMA, the data clock rate is set at 1.5 GHz. An external clock signal provided by an HP83620 synthesizer followed by a frequency divider reduces the clock jitter from the FPGA board [11]. An HP8565E spectrum analyzer is used to record the output signal spectrum for calculating SINAD, and an HP7082A digital sampling oscilloscope is used to measure the signal voltage.

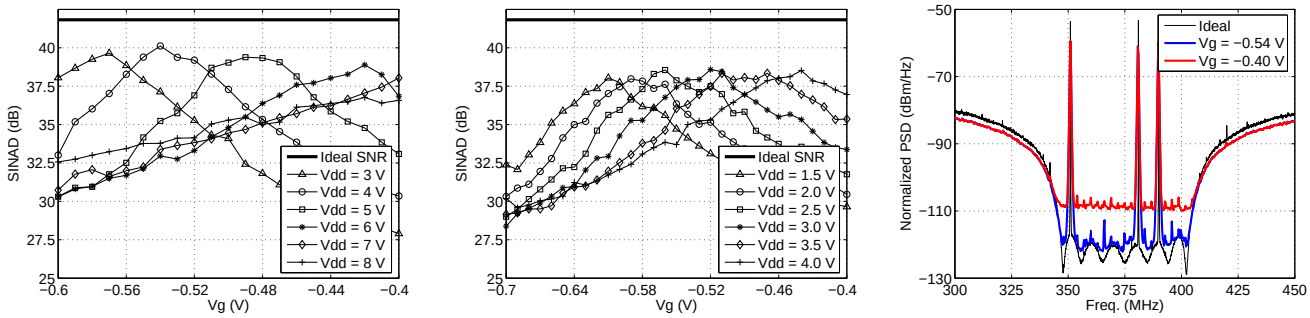
A bandpass filter is inserted between the output of the converter and the spectrum analyzer to reduce the out-of-band noise. The filter is chosen to be absorptive to eliminate reflections from the load, which cause additional nonlinear ISI. A lossy filter is not the right choice for an integrated DAC, and it is used here only for characterization purposes. A terminated bridge balun circuit is used for the differential converter measurements (dashed box in Fig. 12). Single-ended converters were measured by using half of the differential converter and biasing the other half at cutoff. All the measurement results are taken with a three-tone $\Delta\Sigma$ test signal at a 1.5 GHz clock frequency with 60 MHz possible signal bandwidth centered at 375 MHz.

V. Driver Measurement and Simulation Results

A. Converter Linearity Measurements and Simulations

The measured SINAD for the resistively biased single-ended converter at different gate and drain bias voltages is shown in Fig. 13(a). The ideal calculated value of the testing $\Delta\Sigma$ signal is 41.8 dB. It can be seen that the measured SINAD is very sensitive to the transistor gate and drain supply voltages, V_g and V_{dd}. Measured SINAD for the inductively biased single-ended converter is shown in Fig. 13(b), where similar dependence on bias is seen. As an example, Fig. 13(c) shows the relative signal power spectral density (PSD) for the best and the worst cases when $V_{dd} = 4\,\text{V}$. It can be seen that the SINAD drop is directly related to the increase in the in-band noise floor caused by nonlinear ISI. Comparing Fig. 13(a) and (b), the best achievable SINAD for the inductively biased single-ended converter is slightly worse than for the resistively biased case. We believe that this is due to the frequency dependence of the inductive bias circuit, which causes extra load reflection to the switching transistor.

As described in Section II, the switching conductance $g_S(t)$ can cause nonlinear ISI in a single-ended one-bit converter.



(a) (b) (c)

Fig. 13. Measured SINAD at different gate and drain bias voltages for resistively biased (a) and inductively biased (b) singled-ended converters. (c) Measured output signal PSD of the resistively biased single-ended converter at $V_g = -0.54\,\mathrm{V}$ (the best measured SINAD) and $V_g = -0.40\,\mathrm{V}$ (the worst measured SINAD) when $V_d = 4\,\mathrm{V}$. (Signal PSD is normalized to a 1 V peak value waveform, and measured with a 300 kHz IF bandwidth.)

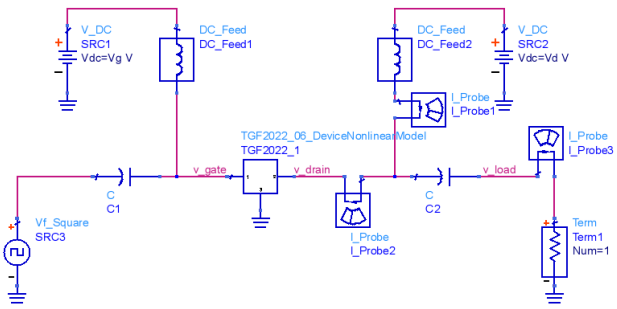
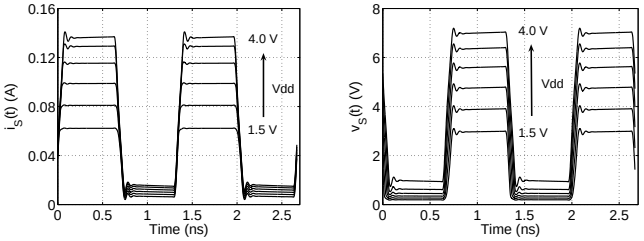


Fig. 14. Agilent ADS circuit diagram used for harmonic balance simulation.



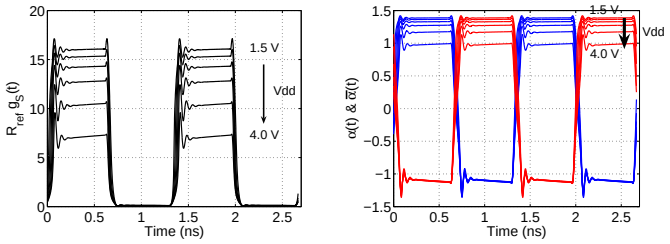
(a) (b)

Fig. 15. Simulated current (a) and voltage (b) waveforms across the transistor at $V_g = -0.50\,\mathrm{V}$ for different V_{dd} voltages.

The waveform $g_S(t)$ is directly affected by the gate and drain supply voltages, as a result, the SINAD is a function of V_g and V_{dd}, as measured in Fig. 13(a) and (b).

In order to relate theoretical and measured results, harmonic balance simulations are done with the Agilent ADS circuit simulator as in the diagram shown in Fig. 14. A Materka nonlinear model was made available by TriQuint for the TGF2022-06 pHEMT transistor. The harmonic-balance solver is a frequency domain technique used for nonlinear analysis at microwave frequencies, and has difficulty converging for the extremely long $\Delta\Sigma$ signals. For the three tone test signal used here the sequence has a minimum of 1 million bits. Since a $\Delta\Sigma$ modulated signal has approximately equal numbers of $+1$ and -1 bits, a periodic signal with alternate $+1$ and -1 bits at 1.5 GHz clock frequency is chosen for the simulation.

Using the transistor nonlinear model does not allow us to separate g_S from the capacitance as was done in the theoretical model of Fig. 5. However, for this device the



(a) (b)

Fig. 16. Simulated $R_{ref}\,g_S(t)$ (a) and $\alpha(t)$ (blue curve) & $\overline{\alpha}(t)$ (red curve) (b) waveforms at $V_g = -0.50\,\mathrm{V}$ for different V_{dd} voltages.

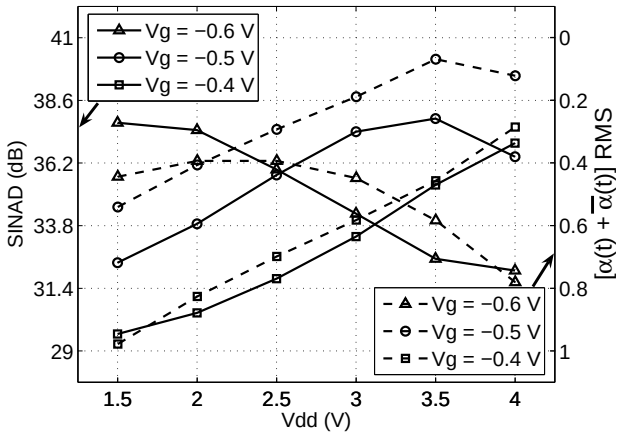
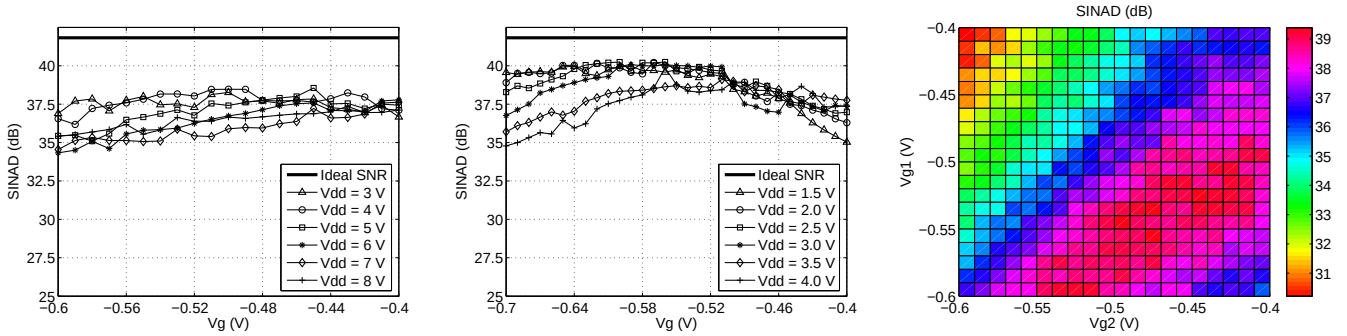


Fig. 17. Measured SINAD (solid line) and simulated RMS value (dashed line) of $\alpha(t) + \overline{\alpha}(t)$ at different bias conditions.

output capacitance is small and on the order of 0.1 pF. So the switching conductance $g_S(t)$ can be approximated by using the simulated current and voltage waveforms across the transistor, shown in Fig. 15. From these simulated results, the normalized switching conductance $R_{ref}\,g_S(t)$ and parameters $\alpha(t) = \ln\left(R_{ref}\,g_S(t)\right)/2$ and $\overline{\alpha}(t)$ are calculated and compared with the theoretical results in Section II. Taking $R_{ref} = 50\,\Omega$, which is the input impedance of instruments used in the measurement, resulting waveforms are plotted in Fig. 16.

In Section II, $\alpha(t) + \overline{\alpha}(t) = 0$ was determined to be the condition when no nonlinear ISI is generated by the transistor switching conductance. Fig. 17 shows that the simulated RMS value of $\alpha(t) + \overline{\alpha}(t)$ at various bias conditions can be used as an indicator of nonlinear ISI contributed by the transistor in



(a) (b) (c)

Fig. 18. Measured SINAD at different gate and drain bias voltages for resistively biased (a) and inductively biased (b) differential converters. (c) Measured SINAD of the resistively biased differential converter at $V_{dd} = 3\,\mathrm{V}$ and different gate bias voltages V_{g1} and V_{g2}.

Fig. 5(a). This performance measure roughly agrees with the measured SINAD results provided for comparison. At $V_g = -0.6\,\mathrm{V}$ and $V_{dd} < 2.5\,\mathrm{V}$, the transistor is in the deep cutoff region, and the model is limited.

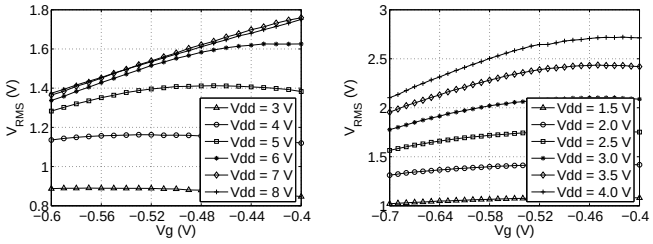
The differential converter SINAD results compared to the single-ended ones are much less sensitive to the transistor gate bias voltage, as shown in Fig. 18(a). This agrees with the conclusion from the theoretical derivation in Section III, that the differential driver output signal linearity is less dependent on $g_S(t)$. However, we also notice that the best SINAD at different drain supply voltages for the resistively biased differential converter is worse than in the single-ended case. This is due to component mismatch in the differential pair.

By adjusting the gate biases of two transistors in the differential pair, improved SINAD results can be obtained, as shown in Fig. 18(c). This is effectively an external control method to equalize $g_{S1}(t)$ and $g_{S2}(t)$, showing that having matched components is very critical in the differential converter implementation. Compared to the single-ended case, the SINAD of the inductively biased differential converter in Fig. 18(b) shows not only less sensitivity to the transistor gate bias voltage but also better linearity, since the even-order nonlinear ISI effects caused by the time-varying conductance of the transistor and the drain bias inductor are reduced in the differential configuration.

B. Converter Efficiency Measurement Results

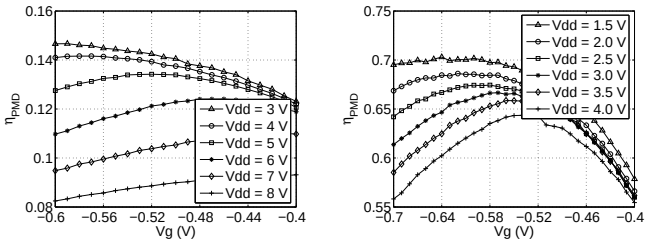
The measured single-ended converter output signal RMS voltages at different bias conditions are shown in Fig. 19. The relative pulse-modulation drain efficiency η_{PMD} as defined in the previous section is plotted in Fig. 20. As expected, the inductively biased converter has a high efficiency in the range of 55-75%. The major loss factor in the resistively biased converter is the current through the bias resistor, and its ideal predicted pulse-modulation drain efficiency is only 16.67%, as in Fig. 11(a).

For both cases, the measured efficiencies are lower than predicted by theory, in part due to the switching loss in the transistor. In addition, the input signal is too low for large drain biases, as can be seen from the saturation of V_{RMS} results in Fig. 19(a). The balun circuit used in the differential measurement setup would require a large bandwidth from a few MHz to 10 GHz (7^{th} clock harmonic) to measure correct



(a) (b)

Fig. 19. Measured V_{RMS} of the single-ended converter at different gate and drain bias voltages: (a) resistively biased, (b) inductively biased.



(a) (b)

Fig. 20. Measured η_{PMD} of the single-ended converter at different gate and drain bias voltages: (a) resistively biased, (b) inductively biased.

waveforms. The balun designed for our measurement only has about 50% fractional bandwidth around 375 MHz, and therefore the output signal waveform of the differential DACs could not be accurately captured by the oscilloscope. Thus, efficiency measurements were not meaningful for the differential converters. However, the results for the single-ended configuration provide an upper bound for the differential case. Ideally, the pulse-modulation efficiencies for both cases should be the same.

VI. Conclusion and Discussion

In summary, this paper presents a detailed theoretical investigation of nonlinear ISI in one-bit $\Delta\Sigma$ modulated RF power DACs. The main results shown by the theory are: (1) as expected, the differential configuration is superior in terms of linearity since odd-mode nonlinear terms are eliminated by symmetry; (2) the advantage of the differential circuit is conditional upon the two switching transistors and all other circuit components being identical; (3) the simpler single-ended DAC circuit linearity is heavily dependent on the time-

varying conductance of the transistor driven as a switch; (4) the parasitic capacitance of the transistor is modeled as part of the load, and larger values of capacitance have a stronger effect on the linearity performance for both architectures; and (5) the bias circuit is included in the theoretical model, and affects the linearity as well.

Experimental validation is performed on single-ended and differential DACs implemented at a center frequency of 375 MHz with a clock at 1.5 GHz for a 50 MHz signal bandwidth containing a three-tone test signal. The experimental data are consistent with the theoretical conclusions discussed above, with the following additional results: (1) the type of bias circuit (resistive or inductive) has a strong effect on both efficiency and linearity, with a broadband inductive bias preferred; and (2) the efficiency and linearity depend on the gate and drain bias conditions. The latter is consistent with the theoretical conclusion and simulation results that the linearity depends on the time-varying conductance of the transistor driven as a switch, since $g_S(t)$ is a function of bias. In addition, by individually biasing the two transistors in the differential circuit, it is possible to externally control the level of mismatch between the two transistors, and thus show quantitatively the linearity degradation due to device parameter mismatch. Matched components can be controlled to a higher level in an integrated circuit, and a GaAs MMIC DAC design is the topic of future work.

Finally, the bandpass filter (Fig. 1(a)) in the load circuit presented in this work is an absorptive topology, which is not a good choice for efficiency, but is convenient for testing since it eliminates reflections. It can be shown, by extending the theory described in this paper, that nonlinear effects added by a low-loss reflective filter can be minimized with proper, but nontrivial, filter design [28]. This is also a topic of a future publication.

In conclusion, the results of this paper provide guidance in choosing switching device and bias circuit design, in order to minimize nonlinear ISI in one-bit power DACs for $\Delta\Sigma$ modulated RF transmitters.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Dan Purdy at ONR for support and helpful inputs, and Luke Sankey from UC Boulder for help with FPGA board programming. We are also grateful for TriQuint Semiconductor for providing the transistor nonlinear circuit model.

APPENDIX

A. Derivation of Equation (27)

Assuming there is no nonlinear ISI from the source, $\rho_S(t)$ and $m(t)$ have the forms

$$\rho_S(t) = \sum_n d(n)u(t-nT),$$
$$m(t) = 1 - \sum_n d(n)u(t-nT).$$

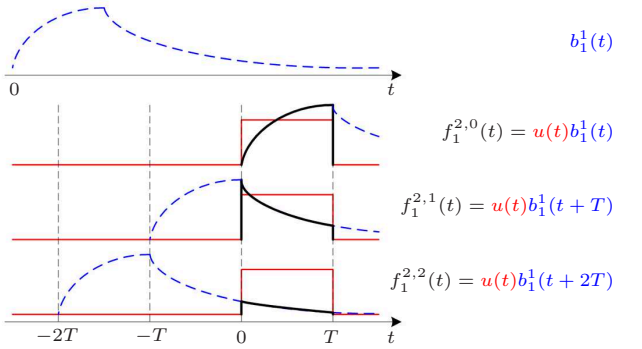


Fig. 21. Unit pulse waveforms of $f_1^{2,m}(t)$. ($b(t)$ dashed line, $u(t)$ thin-solid line, $f(t)$ thick-solid line.)

Substitute the above into (15) and (17). For $k = 0$,

$$i_0^+(t) = \frac{V_{dd}}{2R_{ref}}\left(-1 + \sum_n d(n)u(t-nT)\right)$$

For $k = 1$,

$$i_1^-(t) = \frac{V_{dd}}{2R_{ref}}\left(B_1 + \sum_n d(n)b_1^1(t-nT)\right),$$

where

$$B_1 = \rho_L(t) * (-1) = -\mathcal{R}_L(0),$$
$$b_1^1(t) = \rho_L(t) * u(t).$$

Then from (17), the following is obtained

$$i_1^+(t) = \frac{V_{dd}}{2R_{ref}}\Bigg(\sum_n d(n)f_1^1(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)f_1^{2,m}(t-nT)\Bigg),$$

where the causality of $u(t)$ and $\rho_L(t)$ sets the $m < 0$ terms to zero and

$$f_1^1(t) = u(t)B_1,$$
$$f_1^{2,m}(t) = u(t)b_1^1(t+mT).$$

Fig. 21 illustrates how the unit pulse waveform of each $f_1^{2,m}(t)$ is constructed. Be aware that the term associated with $m = 0$ does not represent a nonlinear ISI effect. For mathematical simplicity, here it is grouped together with terms $m \geq 0$.

Similarly, higher order $i_k^+(t)$ can be expanded as

$$i_k^+(t) = \frac{V_{dd}}{2R_{ref}}\Bigg(\sum_n d(n)f_k^1(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)f_k^{2,m}(t-nT) + \sum_{\ell\geq m}\sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-\ell)f_k^{3,m,\ell}(t-nT) + \cdots\Bigg).$$

Therefore, $i^+(t)$ has the form as in (27).

B. Derivation of Equation (31) and (32)

At the reference plane in Fig. 8(c), as indicated by the dashed line, KCLs in the time and Laplace domains give

$$\begin{aligned}\begin{pmatrix} i_1(t) \\ i_2(t) \end{pmatrix} &= -\begin{bmatrix} g_{S1}(t) & 0 \\ 0 & g_{S2}(t) \end{bmatrix}\begin{pmatrix} v_1(t)+V_{DD1} \\ v_2(t)+V_{DD2} \end{pmatrix}, \\ \begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} &= [Y_t(s)]\begin{pmatrix} V_1(s) \\ V_2(s) \end{pmatrix} + [Y_L'(s)]\begin{pmatrix} V_{DD1}(s) \\ V_{DD2}(s) \end{pmatrix},\end{aligned} \tag{51}$$

where

$$[Y_t(s)] = [Y_L'(s)] + \begin{bmatrix} Y_{b1}(s) & 0 \\ 0 & Y_{b2}(s) \end{bmatrix}.$$

For the steady state response of the circuit, if V_{DD1} and V_{DD2} are ideal DC voltage sources, and because the load circuit is AC coupled to the transistor, (51) can be simplified as

$$\begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} = [Y_t(s)]\begin{pmatrix} V_1(s) \\ V_2(s) \end{pmatrix}.$$

Define even- and odd-mode variables, as in (28) and (29), and the change-of-variable relationship

$$\begin{pmatrix} i_\Sigma(t) \\ v_\Sigma(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix}\begin{pmatrix} i_\Sigma^+(t) \\ i_\Sigma^-(t) \end{pmatrix},$$

$$\begin{pmatrix} i_\Delta(t) \\ v_\Delta(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix}\begin{pmatrix} i_\Delta^+(t) \\ i_\Delta^-(t) \end{pmatrix},$$

Solving for $[i^+(t)]$ and $[I^-(s)]$ respectively,

$$\begin{pmatrix} i_\Sigma^+(t) \\ i_\Delta^+(t) \end{pmatrix} = [\rho_S(t)]\begin{pmatrix} i_\Sigma^-(t) \\ i_\Delta^-(t) \end{pmatrix} - [m(t)]\frac{1}{2R_{ref}}\begin{pmatrix} V_{DD\Sigma} \\ V_{DD\Delta} \end{pmatrix}, \tag{52}$$

$$\begin{pmatrix} I_\Sigma^-(t) \\ I_\Delta^-(t) \end{pmatrix} = [\mathcal{R}_L(s)]\begin{pmatrix} I_\Sigma^+(t) \\ I_\Delta^+(t) \end{pmatrix}, \tag{53}$$

where

$$[\rho_S(t)] = (\mathrm{I} + R_{ref}[g_S(t)])^{-1}(\mathrm{I} - R_{ref}[g_S(t)]), \tag{54}$$

$$[m(t)] = (\mathrm{I} + R_{ref}[g_S(t)])^{-1}\,2R_{ref}[g_S(t)], \tag{55}$$

$$[\mathcal{R}_L(s)] = (\mathrm{I} + R_{ref}[Y_t^{\Sigma\Delta}(s)])^{-1}(\mathrm{I} - R_{ref}[Y_t^{\Sigma\Delta}(s)]), \tag{56}$$

and

$$\begin{aligned}[g_S(t)] &= \frac{1}{2}\begin{bmatrix} g_{S\Sigma}(t) & g_{S\Delta}(t) \\ g_{S\Delta}(t) & g_{S\Sigma}(t) \end{bmatrix}, \\ [Y_t^{\Sigma\Delta}(s)] &= \frac{1}{2}\begin{bmatrix} \sum_{i,j} Y_{tij} & \sum_i (Y_{ti1}-Y_{ti2}) \\ \sum_j (Y_{t1j}-Y_{t2j}) & \sum_{i=j} Y_{tij} - \sum_{i\neq j} Y_{tij} \end{bmatrix}, \\ &= \frac{1}{2}\begin{bmatrix} Y_{b\Sigma}(s)+sC_\Sigma & Y_{b\Delta}(s)+sC_\Delta \\ Y_{b\Delta}(s)+sC_\Delta & Y_{b\Sigma}+sC_\Sigma+4Y_L(s) \end{bmatrix}.\end{aligned}$$

Based on (52) and (53), $[i^+(t)]$ and $[i^-(t)]$ are solved in series as in (31) and (32).

C. Derivation of Equations (47) and (48)

If we define

$$\alpha_1(t) = \frac{\ln(R_{ref}g_{S1}(t))}{2},$$
$$\alpha_2(t) = \frac{\ln(R_{ref}g_{S2}(t))}{2},$$

Equations (39) and (40) are rewritten as

$$m^{cc}(t) = 1 + \frac{1}{2}\left(\tanh\alpha_1(t) + \tanh\alpha_2(t)\right),$$
$$m^{dc}(t) = \frac{1}{2}\left(\tanh\alpha_1(t) - \tanh\alpha_2(t)\right).$$

Based on (55) and (54),

$$[\rho_S(t)] = \mathrm{I} - [m(t)] = \begin{bmatrix} \rho_S^{cc}(t) & \rho_S^{dc}(t) \\ \rho_S^{dc}(t) & \rho_S^{cc}(t) \end{bmatrix},$$

where

$$\rho_S^{cc}(t) = -\frac{1}{2}\left(\tanh\alpha_1(t) + \tanh\alpha_2(t)\right),$$
$$\rho_S^{dc}(t) = -\frac{1}{2}\left(\tanh\alpha_1(t) - \tanh\alpha_2(t)\right).$$

If the transistors switch fast enough, we can define

$$\begin{aligned}\tanh\alpha_1(t) = &-\sum_n u_0(t-nT) - \sum_n d(n)u_1(t-nT) \\ &-\sum_n d(n)d(n-1)u_2(t-nT),\end{aligned}$$

and if the transistors and bias circuits in the differential converter are identical, we have

$$\begin{aligned}\tanh\alpha_2(t) &= \tanh\overline{\alpha_1}(t) \\ &= -\sum_n u_0(t-nT) + \sum_n d(n)u_1(t-nT) \\ &\quad -\sum_n d(n)d(n-1)u_2(t-nT).\end{aligned}$$

Therefore,

$$m^{cc}(t) = 1 - \sum_n u_0(t-nT) - \sum_n d(n)d(n-1)u_2(t-nT)$$
$$m^{dc}(t) = -\sum_n d(n)u_1(t-nT),$$
$$\rho_S^{cc}(t) = \sum_n u_0(t-nT) + \sum_n d(n)d(n-1)u_2(t-nT),$$
$$\rho_S^{dc}(t) = \sum_n d(n)u_1(t-nT),$$

and from (56), the load reflection $[\rho_L(t)]$ is

$$[\rho_L(t)] = \begin{bmatrix} \rho_L^{cc}(t) & 0 \\ 0 & \rho_L^{dd}(t) \end{bmatrix}.$$

Substitute the above expressions for $[m(t)]$, $[\rho_S(t)]$, and $[\rho_L(t)]$ into (33) (34) and (35). For $k = 0$,

$$\begin{aligned}i_{\Sigma 0}^+(t) = \frac{V_{dd}}{R_{ref}}\Bigg(&-1 + \sum_n u_0(t-nT) \\ &+ \sum_n d(n)d(n-1)u_2(t-nT)\Bigg),\end{aligned}$$
$$i_{\Delta 0}^+(t) = \frac{V_{dd}}{R_{ref}}\sum_n d(n)u_1(t-nT).$$

For $k = 1$,

$$i^-_{\Sigma 1}(t) = \frac{V_{dd}}{R_{ref}}\left(B_1 + \sum_n b_1^0(t-nT) + \sum_n d(n)d(n-1)b_1^{2,1}(t-nT)\right),$$
$$i^-_{\Delta 1}(t) = \frac{V_{dd}}{R_{ref}}\sum_n d(n)b_1^1(t-nT),$$

and

$$i^+_{\Sigma 1}(t) = \frac{V_{dd}}{R_{ref}}\left(\sum_n f_1^0(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)f_1^{2,m}(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-1)d(n-m)d(n-m-1) \cdot f_1^{4,1,m,m+1}(t-nT)\right),$$
$$i^+_{\Delta 1}(t) = \frac{V_{dd}}{R_{ref}}\left(\sum_n d(n)f_1^1(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-m-1) \cdot f_1^{3,m,m+1}(t-nT).\right)$$

The higher order $i_k^+(t)$ can be expanded similarly, and by summing all the $i^+_{\Sigma k}(t)$ and $i^+_{\Delta k}(t)$, (47) and (48) are derived.

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